ABSTRACT OF THE DISCLOSURE

An array process diagnosis test structure for an integrated circuit including a transistor array composed of vertical FET memory cell access transistors, which are formed into the depth of a substrate in the form of active webs which run parallel in the lateral direction of the circuit is disclosed. Memory cell storage capacitors in the array test structure are formed in deep trenches on the end faces of those sections of the active webs which form the vertical FET transistors. Word lines are arranged along the webs and along parallel intersecting bit lines of the array, outside of which, and on two mutually opposite edges, are located a first and second word line comb. The wordline combs are offset and connected alternately to different word lines. In addition, a first and a second bit line comb are formed on the two other opposing edges of the transistor array mutually offset and each connected to different bit lines. The test structure provides a convenient means to carry out reliability investigations on the gate oxide of the vertical FET transistors and on the capacitor dielectric in the deep trenches, capacitance measurements between the word lines, and between the word lines and other circuit layers, as well as capacitance measurements between the bit lines and between the bit lines and other circuit layers, and thus facilitates diagnosis of possible fault sources arising during the production process.

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